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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/022,851	12/20/2001	Claude Thibeault	P 276792 P(US)2001-019	1516

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EXAMINER	
GHULAMALI, QUTBUDDIN	
ART UNIT	**PAPER NUMBER**
2637	

DATE MAILED: 09/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/022,851	THIBEAULT ET AL.	
	Examiner	Art Unit	
	Qutub Ghulamali	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *12-20* is/are allowed.

6)☒ Claim(s) *1-11 and 21-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/30/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the reference to state transitions "T1" and "T2" in the specification page 4, sections 00016, 00061) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-11 and 21-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Balakrishnan et al (USP 5,101,347) in view of Tan et al (USP 5,815,031).

Regarding claims 1 and 21, Balakrishnan discloses a system (transmitter and receiver) of data transmission comprising:

receiving a plurality of sets of input signals (multiple data slices), each input signal having a series of state transitions (figs. 2-3; series of data characters) synchronized to a data clock signal having a period T CLK (col. 3, lines 13-48); and

transmitting a corresponding plurality of sets of output signals such that each output signal (1) corresponds to an input signal of the corresponding set (col. 3, lines 13-25; col. 4, lines 33-40), (2) passes along a corresponding one of a plurality of conductive paths (parallel data bus), and (3) has a series of state transitions corresponding to the series of state transitions of the corresponding input signal (col. 3, lines 35-60), wherein a time between a state transition on an input signal of one set and the corresponding state transition on the corresponding output signal exceeds a time between a state transition on an input signal of another set and the corresponding state transition on the corresponding output signal by a delay period T DLY, and

wherein the period T CLK is greater than the delay period T DLY (col. 2, lines 10-39). Balakrishnan, however, does not explicitly disclose, "adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries an output signal of another set". Tan in a similar field of endeavor discloses an improved signal routing scheme includes a plurality of dynamic signal lines disposed in parallel to each other wherein adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries an output signal of another set (col. 2, lines 32-44, 53-60). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use plurality of dynamic signal lines parallel to each other (adjacent conductive paths) separated by conductive path to carry output signal of another set as taught by Tan in the system of Balakrishnan because it can mitigate crosstalk noise by reducing unwanted coupling between signal paths.

Regarding claims 2, 30, Balakrishnan discloses the delay period T_DLY is at least as long as a rise time of the data clock signal (fig. 3).

Regarding claims 3 and 22, Balakrishnan discloses each state transition of an output signal corresponds to a different one among the state transitions of the corresponding input signal (col. 3, lines 13-28).

Regarding claims 4, 23 and 33, Balakrishnan discloses the plurality of conductive paths can be fabricated on a semiconductor substrate, and wherein said receiving and said transmitting occur on the semiconductor substrate (col. 4, lines 3-18).

Regarding claims 5, 6, 7, 24, 25, 26 the parameters; length, distance between adjacent conductive path, and width of the conductive path are design issues (features) related to

achieving the desired delay in a high speed signal communication and well known in semiconductor fabrication industry for achieving desired objectives in reducing the skew effects between parallel data paths, such as disclosed by Nomura (USP 6,128,347) (figs. 16, 17A-C).

Regarding claims 8 and 28, Balakrishnan discloses each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines (col. 3, lines 35-60); and

wherein said method further comprises coupling the data clock signal to one of the plurality of transmission lines (fig. 2; col. 3, lines 22-28).

Regarding claims 9, 29, Balakrishnan discloses each one among the plurality of conductive paths includes a corresponding one of a plurality of buffers (storage locations) (col. 3, lines 35-48).

Regarding claims 10, 31, Balakrishnan discloses,

transmitting each output signal among a first one of the plurality of sets of output signals includes latching the series of state transitions of the corresponding input signal onto the output signal in response to a first clock signal, and wherein transmitting each output signal among a second one of the plurality of sets of output signals includes latching the series of state transitions of the corresponding input signal onto the output signal in response to a second clock signal (fig. 2, col. 3, lines 13-48, 54-67).

Regarding claims 11 and 32, Balakrishnan discloses the first and second clock signals are based on the data clock signal, and wherein a time between a state transition on the data clock signal and a corresponding state transition on the second clock signal exceeds a time between a

state transition on the data clock signal and a corresponding state transition on the first clock signal by the delay period T DLY (col. 2, lines 10-39).

Regarding claim 34, Balakrishnan discloses a data receiver configured and arranged to receive the plurality of first output signals and the plurality of second output signals and to produce a plurality of first received signals and a plurality of second received signals (col. 4, lines 20-54), wherein each among the plurality of first received signals corresponds to one among the plurality of first output signals, and each among the plurality of second received signals corresponds to one among the plurality of second output signals (col. 3, lines 13-25; col. 4, lines 33-40), and wherein each of the first and second received signals has a series of state transitions corresponding to the series of state transitions of the corresponding output signal (col. 2, lines 10-39), and wherein the state transitions of each of the first and second received signals are synchronized to a received data clock signal, and wherein one among the rising and falling edges of the data clock signal is synchronous with the other among the rising and falling edges of the received data clock signal (col. 3, lines 61-67).

Allowable Subject Matter

4. Claims 12-20 allowed.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patents:

Nomura (USP 6,128,347) discloses signal transmission circuit with protection line driven with signal having same phase as transmission signal to mitigate crosstalk.

Schipper et al (USP 6,128,337) shows a multi-path signal discrimination method.

Lincoln (US Pub. 2005/0069041) shows a coherent expandable high speed interface.

Umemura et al (USP 6,600,790) discloses a gap-coupling bus system.

Malerevich et al (USP 6,611,538) shows a data transmission synchronization system.

Pitroda et al (USP 4,627,047) discloses an integrated voice and data telecommunication switching system.

US Publications:

Bishop, J.A.; Hashemi, M.M.; Kiziloglu, K.; Larson, L.; Dagli, N.; Mishra, U. "Monolithic coaxial transmission lines for mm-wave Ics", High Speed Semiconductor Devices and Circuits, Proceedings IEEE, 5-7 August 1991 Page(s) 252 – 260.

Mikazuki, T.; Matsui, N., "Statistical design techniques for high-speed circuit boards with correlated structure distributions", Components, Hybrids, and Manufacturing Technology, IEEE Transactions on, Volume 14, Issue 3, Sept. 1991 Page(s) 512 – 517.

Mizuno, M. et al; "Clock distribution networks with on-chip transmission lines", Interconnect Technology Conference, Proceedings IEEE 2000 International, 5-7 June 2000 Page(s) 3 – 5.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Qutub Ghulamali whose telephone number is (571) 272-3014. The examiner can normally be reached on Monday-Friday from 8:00AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on (571) 272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QG.
August 31, 2005.

JAY K. PATEL
SUPERVISORY PATENT EXAMINER